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A Survey on Improved Router Design

Shwetha K S[1], Shobha M S[2,] Nandini Byahatti [3]

[1,2]*Assistant Professor, Dept. of Information Science & Engineering, New Horizon College of Engineering, Bangalore, India*
[3]*Student, MTech (Software Engineering), NHCE, Bangalore, India*

Abstract - Networks-on-Chip (NoCs) is an emerging technology and whose accepted solutions cope with the increasing communication requirements in multi-core architectures. NoC provides a very good improvement for the issues like scalability, productivity, power efficiency and signal integrity challenges of complex system-on-chip(SoC) design. In this paper, we have survey on few of the techniques and methodologies to improve the router performance by reducing power consumption, by reducing excess wastage of bandwidth, by dynamically assign VCs to VNETs to significantly reduce the number of physical buffers in routers depending on VNET load, by a reliable NoC router architecture which is capable of tolerating multiple permanent faults etc.

Keywords: Router, Network-on-chip, Buffer. system-on-chip(SoC)

I.INTRODUCTION

Improving a router performance is very essential part of an industry.many commonly used techniques which increases the performance are by consumes less power, low latency, high reliability, better traffic management, etc. there are many approaches which helps in achieving high performance of a router.

One of the approach is through an emerging technology called networks-on-chip. Other approaches like zero-time wake up for line cards to reduce power consumption and also a technique to reduce retransmission cost of corrupt data by introduction of buffers is also included in the survey.

II. LITERATURE SURVEY

A. Reconfigurable Router Design for Network-On-Chip

If a NoC's router has a larger FIFO buffer, then throughput will be larger and latency will be smaller. But if there is increase in buffer size then there will be increase the power dissipation [1]. So we cannot increase the buffer size a lot. And also with small FIFO latency will be larger. The proposed solution for this is use of reconfigurable heterogeneous routerarchitecture.With reconfiguration technique, it is possible to dynamically change the buffer size to each channel,based on the need of the application and thus power efficiency of the system is increasedincreasing the power efficiency of the system.

The working of the proposed router architecture can be explained using an example [2]. Consider we have a router with buffer size equal to 4. The router needs to be configured as: S Channel with buffer size 9, E Channel with buffer size 2, W Channel with buffer size 1, and N Channel with buffer size 4. So the S Channel needs to borrow buffer slots from its neighboring channels. The E Channel occupies two of its four slots. So this channel can lend two slots to its neighbor. As the W Channel occupies only one of its four slots, the three missing slots can be lent to the S Channel. When the S Channel has a flit stored in the E Channel, this flitmust be sent to the output. That means it is passed from the E Channel to the S Channel (d_ E _S), and the flit is directly sent to the output of the S Channel (dout_ S) by a multiplexer. So the S Channel has the following outputs: Its own output (dout _S) and two more outputs (d _S_ E and d _S_ W) to send the flits stored in its channel but belonging to neighbor channels. Router buffer algorithm is used to define buffer size.

B. Optimized Core-links for Low-latency NoCs

In recent years in many-core architectures, the number ofcores has been steadily increasing and thus the network latencybetween cores becomes an important issue for parallel applicationprograms [3]. The new proposed model helps in solving this issue.Network-on-Chip that adds links between randomly-selected routers on a regular router topology is effective for reducing the network latency.

Tile-based on-chip networks consist of $a \times b$routers andcores, which can support multiple network interfaces.Here in this design end-to-end network latency is reduced among coreson a NoC by connecting a core directly to multiple routers using the core-links.

The multiple core-link topologies satisfy the conditions that (i) each core has x core-links, which areconnected to different routers, and that (ii) each router alsohas x ports that are used for connecting different x cores.

For the optimization approach, Genetic Algorithm (GA) is taken here. This is because the problem of generating a graph that has the smallest maximum and average shortest path lengths is known as an NP-hard problem; thus an exhaustive approach is not feasible. By using GA, we can provide the best tradeoff between the core-link length and the number of hops [4].

C. An Improved Router Design for Reliable On-Chip Networks

A permanent fault continues to affect the operation of a circuit from the time of its inception. Electro migration [5], Hot carrier degradation [6] and Time Dependent DielectricBreakdown [7] are typical sources for permanent faults.

Proposedreliable NoC router model is capable of bearing multiple permanent faults. This router provides a better reliability without incurring too much areaand power

overhead as compared to the other baseline NoC routeror other fault-tolerant routers.
This is achieved as follow the new model is designedby making minimal architectural modifications to the 4- stage pipeline of a baseline NoC router which has 4 sages. The architectural modifications involve adding extra circuitry to individual pipeline stages of a NoC router and taking advantage of the inherent redundancy thereby enabling each pipeline stage to tolerate a single permanent fault. Assuming that each individual pipeline stage is affected by only **one** permanent fault, the protected router pipeline will be able to tolerate**four**permanent faults. It can be extended to any number of faults.

D. CUTBUF: Buffer Management and Router Design for Traffic Mixing in VNET-basedNoCs

Networks-on-Chip (NoCs) is an accepted solution to cope with the increasing communication requirements in multi-core architectures. However, the huge amount of design parameters to be considered, i.e. buffer depth, number of VCs, pipeline organization, flit size and so on, makes the NoC design complex. Router buffers are recognized as those that mostly affect the overall behavior of the on-chip network and, consequently, the performance of the whole chip. Moreover, buffers consume a significant part of the NoC router power and storing a packet in a buffer consumes far more energythan its transmission [8]. Besides, the area occupied byan on-chip router is dominated by the buffers [9], [10].
Power consumptionof power in the NoC directly depends on the number of queues. So here we have conflicting goals: reducingthe queues for the power consumption without compromisingthe performance or even the correct systembehavior.
CUTBUF is a proposed router design for virtualchanneled NoCs which allows to dynamically allocateVCs(virtual channels) to VNETs(virtual networks) depending on their actual loads. Thesame buffer can be used to store messages of differenttypes at different points in time, thus which allows resourcereuse and also this architecture efficiently make use of memory. The final goal is to reduce the NoC router areaand power consumption, while minimizing the bad or negative impact on the performance.
It address the reuse of virtual channels (VCs) by mixing the traffic belonging to different VNETs at run-time with a per packet granularity, while avoiding deadlock at both routing and protocol levels.

E. Towards Zero-Time Wakeup of Line Cards in Power-Aware Routers

To save the power consumption many vendors put the line cards in sleep mode when they are idle and wakes up the line card when it has to process assuming that in sleep mode it will consume less power but the fact is linecards will take minutes to come online or wakeup,This entirely diverted the previous assumption that a line card costs zero time to wake up in recent studies, causing the inapplicability of many power-saving schemes to address this issue proposed model gives solution as below..
It keeps the host processor in a line card standby, which only consumes a small fraction of power but will save considerable wakeup time, and also it downloads a slim slot of popular prefixes with higher priority, so that the line card will be ready for forwarding most of the traffic much earlier.
A line card in a high-end commercial router usually spends 4–10 minutes to be ready to efficiently forward packets once it is powered on [11].To support fast line card wakeup, proposed line card architectureprovides penetrating measurement on the boot procedure of line cards. Based on the observations, proposed corresponding designs including separating the on-board CPU power supply from the other parts of a line card, setting up a minimized hardware configuration first by prioritizing prefix download.

F.Bandwidth Efficient Router Design withIntroduction of Buffering to Reduce Retransmission Cost of Corrupt Data

The buffering isfundamental for packet-switching networks [12]. Packets are transmitted through one host to another host, and in between, if some packets are corrupted or lost in any router than it demands the packets from transmitting host which results in loss of bandwidth and time. Retransmission request from a receiver can also lead to sender and network overload.
A new design of router is proposed to reduce an excessive wastage of bandwidth due to retransmission of corrupt or lost packets. In proposed model a buffer is attached to each router. All the packets that pass through a router are saved in the buffer for a very small amount of time. In case if a packet is found corrupt or lost at any router at any given point of time, it can be requested from the previous router which has a correct copy of the packet in its buffer. In this way the wastage of excess bandwidth for retransmission of corrupted or lost packets from sender to receiver is saved.In case of any corrupt packet, the extra bandwidth required for retransmission is limited to a single hop only.

III.CONCLUSION

There is need to improve in router architecture in order to achieve better networking system which includes reduced latency, reduced power consumption, proper usage of bandwidth, permanent fault tolerance etc. in the above survey many techniques have been listed in order to achieve better performance.
And there is always scope for improvement in these models like improving number of permanent fault tolerance, and also attaching buffer to every router which is overhead can be overcome in any alternative ways so on.

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